Analysis of AMD HW-Assisted vIOMMU Implementation and Performance

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Agenda

- AMD HW-vIOMMU Overview
- Software Prototype
- Benchmarks & Performance Analysis
- Summary
AMD HW-vIOMMU
Overview
AMD IOMMU DMA-Remap

- Data structures
  - Device table
  - Command buffer
  - Event log

- Two types of IOMMU page table
  - Host IO Page-table (v1)
    - IOMMU-specific
    - E.g. VFIO (GPA -> SPA)
  - Guest IO Page-table (v2)
    - x86-compatible
    - E.g. DMA APIs (GVA -> GPA)

- 3 modes of operation
  - V1 only
  - V2 only
  - V1 + V2 (nested)
Guest vIOMMU Support

- **Usage cases**
  - Guest IO-protection
  - Shared Virtual Memory (SVM)
  - DPDK support inside VMs

- **SW-based vIOMMU**
  - Need to intercept and emulate MMIO registers behavior
  - Handling guest I/O page table map/unmap/invalidation

![Diagram showing guest view and hardware view of vIOMMU support](image)

- **Diagram elements**
  - QEMU
  - vCPU
  - Guest memory
  - ixbge
  - vIOMMU
  - GPA
  - SPA
  - GIOVA
  - Guest I/O page table
  - Host I/O page table

- **Legend**
  - Pass-through
  - on real hardware
  -_allocated on host
VirtIO-IOMMU

- Virtio-based IOMMU device that offers DMA management for PCI end-point devices
  - Vendor independent virtual IOMMU design
  - Virtual queue design for requests and events
  - Provide basic commands for IOMMU management
    - ATTACH/DETACH
    - MAP/UNMAP
  - No need for TLB invalidation command
  - Require para-virtualized driver in the guest VM
### HW-Assisted vIOMMU (HW-vIOMMU)

- Provides a virtual IOMMU for guest VMs, targeting at PCI pass-through devices

- Required for DMA to SEV-SNP (Secure Nest Paging) Guest

- Improve performance on guest IOMMU via
  - HW-virtualized **guest IOMMU commands**
  - HW-virtualized **MMIO registers**
    - Head / Tail pointers
  - HW-virtualized **Event and PPR logs**
  - **Nested IO page-table**

- Nested IO page-table
  - Guest (v2) table for gIOVA -> GPA
    - Managed by guest IOMMU driver
  - Host (v1) table for GPA -> SPA
    - Managed by VFIO driver
Software Prototype
QEMU Changes

- New amd-viommu device model

- PCI topology b/w vIOMMU and PT devices
  - Each PCI pass-through device must be associated with the corresponding amd-viommu instance

- New guest ACPI IVRS table
  - To support additional IVHD blocks for the new amd-viommu device model

```
qemu-system-x86_64 -machine q35 \
  -device ioh3420,bus=pcie.0,addr=1c.0,multifunction=on,port=1,chassis=1,id=root.1 \ 
  -device amd-viommu,host=0000:00:00.2,id=0 \ 
  -device vfio-pci,host=0000:01:00.0,iommu-id=0 \ 
  -device vfio-pci,host=0000:02:00.0,iommu-id=0 \ 
  -device amd-viommu,host=0000:40:00.2,id=1 \ 
  -device vfio-pci,host=0000:42:00.0,iommu-id=1
```
Host IOMMU Driver Changes

- **Boot-time initialization**
  - Logic for detect and enable vIOMMU feature
  - Allocate commonly used data structure:
    - Domain ID table
    - Device ID table
    - CmdBuf dirty status table

- **Per-VM initialization**
  - Allocate per-vm data structure:
    - Guest MMIO registers
    - Guest Cmd buffer
    - Guest Evt log
  - Host-to-Guest DevID and DomID mappings
  - Trap guest access to 1st 4K of MMIO region (control)

- **Support new IOMMU commands and events**
QEMU & Host IOMMU Driver Interface

- Introduce new device FS
  - /dev/amd-viommu

- Introduce vIOMMU-specific IOCTL interfaces

<table>
<thead>
<tr>
<th>Category</th>
<th>IOCTL Commands</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VM</td>
<td>• VIOMMU_VM_INIT</td>
<td>Setup/destroy per-vm vIOMMU data structure (e.g. Guest MMIO, CmdBuf Dirty Status, Guest Cmd, PPR)</td>
</tr>
<tr>
<td></td>
<td>• VIOMMU_VM_DESTROY</td>
<td></td>
</tr>
<tr>
<td>Device</td>
<td>• VIOMMU_DEVICE_ATTACH</td>
<td>Setup/destroy DevID Mapping Table</td>
</tr>
<tr>
<td></td>
<td>• VIOMMU_DEVICE_DETACH</td>
<td></td>
</tr>
<tr>
<td>Domain</td>
<td>• VIOMMU_DOMAIN_ATTACH</td>
<td>Setup/destroy DomainID Mapping Table</td>
</tr>
<tr>
<td></td>
<td>• VIOMMU_DOMAIN_DETACH</td>
<td></td>
</tr>
<tr>
<td>MMIO</td>
<td>• VIOMMU_MMIO_ACCESS</td>
<td>Handle the trapped guest MMIO access</td>
</tr>
<tr>
<td>Command buffer</td>
<td>• VIOMMU_CMDBUF_MAP_UPDATE</td>
<td>Communicate the guest command buffer address to the host vIOMMU driver to setup GPA → SPA mapping in the host I/O page table</td>
</tr>
<tr>
<td>GCR3</td>
<td>• VIOMMU_GCR3_TABLE_UPDATE</td>
<td>Communicate when guest IOMMU driver update the GCR3 table with pointer to guest page table</td>
</tr>
</tbody>
</table>
Guest AMD IOMMU Driver Changes

- For nested IO page table, guest IOMMU driver programs GIOVA -> GPA in the IOMMU guest page table.
  - VFIO programs GPA -> SPA in the IOMMU host page table.
  - IOMMU hardware walks through guest + host table to translate GIOVA -> SPA when receive DMA request.

- New IOMMUv2 page table support for DMA-API
  - Use the generic IO page table framework
  - Add command line option "amd_iommu_iova=[v1 (default)|v2]"
  - Use PASID=0 (for io-protection mode)
  - https://lore.kernel.org/patchwork/cover/1394015

From: 48882—AMD I/O Virtualization Technology (IOMMU) Specification
Benchmarks & Performance Analysis
Goals

- Compare PCI device pass-through performance of AMD HW-vIOMMU with other vIOMMU solutions.

- Analyze AMD HW-vIOMMU performance data and identify room for improvement.
Configurations

- **Bare-metal + No IOMMU**
  - Host Kernel: v5.12 (iommu=pt)

- **VM + PT:**
  - **No Guest IOMMU**
    - Host Kernel: v5.12
    - Guest Kernel: v5.12
    - Qemu: v6.0
  - **AMD HW-vIOMMU**
    - Host Kernel: v5.12 with vIOMMU support
    - Guest Kernel: v5.12 with io-pagetable support for IOMMUv2 page table
    - Qemu: v6.0 with AMD vIOMMU device model
  - **VirtIO IOMMU**
    - Host Kernel: v5.12
    - Guest Kernel: v5.13-rc4 with x86 virtio-iommu
    - Qemu: v6.0 with VirtIO IOMMU device model
- Samsung SSD 960EVO (m.2)
- Intel SSD DC P3700 Series (u.2)
- Use the same Linux NVME driver
- Use default configurations for OS and benchmark

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Intel Read (MB/sec)</th>
<th>Intel Write (MB/sec)</th>
<th>Samsung Read (MB/sec)</th>
<th>Samsung Write (MB/sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bare Metal (no IOMMU)</td>
<td>331.82</td>
<td>1512.4057</td>
<td>327.60</td>
<td>376.48</td>
</tr>
<tr>
<td>PT (no IOMMU)</td>
<td>318.38</td>
<td>1049.42</td>
<td>321.04</td>
<td>374.89</td>
</tr>
<tr>
<td>PT + HW-vIOMMU</td>
<td>230.88 (72.5%)</td>
<td>218.66 (20.8%)</td>
<td>228.82 (72.3%)</td>
<td>240.33 (64.1%)</td>
</tr>
<tr>
<td>PT + VirtIO IOMMU</td>
<td>136.02 (42.7%)</td>
<td>127.70 (12.2%)</td>
<td>132.04 (41.1%)</td>
<td>127.56 (34.0%)</td>
</tr>
</tbody>
</table>

fio --thread --size=100% --direct 1 --buffered 0 --iodepth 8 --invalidate 1 --bs 4096 --ioengine libaio --time_based --norandommap --random_generator=lfsr --cpus_allowed_policy=split --exitall --ramp_time 5 --runtime 60 --allrandrepeat 0 --rw rand[read|write]
NETPERF : TCP_STREAM

- Intel 82599ES 10GbE
  - Dual ports
  - Physical loop-back mode
- Linux ixgbe driver
- Use default configuration for benchmark and OS
- Use PT (no IOMMU) case for base-line

<table>
<thead>
<tr>
<th>Intel 10GbE</th>
<th>Send (Gbps) Min / Avg / Max</th>
<th>Receive (Gbps) Min / Avg / Max</th>
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</thead>
<tbody>
<tr>
<td>PT (no IOMMU)</td>
<td>9.4</td>
<td>9.4</td>
</tr>
<tr>
<td>PT + HW-vIOMMU</td>
<td>7.78 (84.47%)</td>
<td>9.4</td>
</tr>
<tr>
<td></td>
<td>7.86 (83.68%)</td>
<td></td>
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<td></td>
<td>8.01 (82.77%)</td>
<td></td>
</tr>
<tr>
<td>PT + VirtIO IOMMU</td>
<td>1.91 (20.31%)</td>
<td>9.4</td>
</tr>
<tr>
<td></td>
<td>2.25 (23.93%)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.44 (25.96%)</td>
<td></td>
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NETPERF : TCP_STREAM

- Mellanox MT28800 100GbE
  - Dual port
  - Physical loop-back mode
- Linux mlx5_core driver
- Default configuration

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<td>Min / Avg / Max</td>
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<td>PT (no IOMMU)</td>
<td>8.66 / 22.24 / 38.54</td>
<td>19.89 / 21.80 / 24.55</td>
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<tr>
<td>PT + HW-vIOMMU</td>
<td>7.61 (34.1%) / 8.79 (30.0%) / 9.70 (25.0%)</td>
<td>8.02 (40.3%) / 10.65 (48.8%) / 15.05 (61.3%)</td>
</tr>
<tr>
<td>PT + VirtIO IOMMU</td>
<td>3.10 (13.9%) / 3.85 (13.8%) / 5.00 (12.9%)</td>
<td>5.63 (28.3%) / 9.34 (42.8%) / 12.32 (50.2%)</td>
</tr>
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</table>
NETPERF : TCP_STREAM (Intel vs Mellanox)

For Netperf, AMD HW-vIOMMU performance bottleneck:
- Send : 8Gbps
- Receive : 10Gbps

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PT + vIOMMU Overhead Analysis

- Guest INVALIDATE_IOMMU_PAGES
  - Instruct IOMMU to invalidate range of entries in TLB

- IOMMU TLB misses
  - Perf stat w/ IOMMU performance counters (host)
  - Large amount of IOMMU TLB miss PTE/PDE in vIOMMU case
  - No IOMMU TLB miss in PT case, since only use the IOMMU host page table (pinned)

- Nested page table walk
  - Higher latency than non-nested page table walk
Summary

- AMD HW-vIOMMU shows improvement of PCI pass-through I/O performance for guest IO-protection use case, when comparing to other SW-vIOMMU solutions

- Improvements:
  - Better IOMMU TLB invalidation scheme to reduce the number of:
    - IOMMU invalidations
    - Number of page-table walks

- Next Steps
  - Upstreaming to Linux / Qemu
  - Experiment w/ other vIOMMU usecases
  - Solution for hybrid vIOMMU model (SW+HW vIOMMU)
  - Interrupt Remapping support w/ HW vIOMMU
Thank you
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