Scalable Work Submission in Device Virtualization

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Agenda

- Scalability in Device Virtualization
- ENQCMD Instruction
- ENQCMD Virtualization
- Example - SVA work submission
Scalability In Device Virtualization

### PCIe* SRIOV

- **PF**
  - **VF (DWQ)**
  - **VF (DWQ)**
  - **VF (DWQ)**
  - **VF (DWQ)**

  Device

- **VM 0**
- **VM 1**
- **...**
- **VM n**

### Intel® Scalable IOV

- **VM 0**
- **VM 1**
- **...**
- **VM n**

- **VDEV 0**
- **VDEV 1**
- **...**
- **VDEV n**

- **ADI (DWQ)**
  - **ADI (DWQ)**
  - **ADI (DWQ)**
  - **ADI (DWQ)**

  Device

- **PF**
  - **VF (DWQ)**
  - **VF (DWQ)**
  - **VF (DWQ)**

- **VM 0**
- **VM 1**
- **...**

**Key Points:***

- **Dedicated work queue (DWQ)** implemented in VFs and ADIs
- **Provide Scalability by hard partitioning the hardware resources**
- **Difficult to increase VFs / ADIs due to limited resources on some devices**
Shared Work Queue

- Typical usage: Shared Virtual Addressing (SVA)
  - Device uses the CPU virtual address for DMA

- Distinguish the context of different workloads by Process Address Space ID (PASID)

- DMA address translation at Requestor ID (RID) + PASID granularity per IOMMU
- Allow sharing the same device interface by users in VMs and Host
- No hard limitation on user number
- Device can implement DWQ and SWQ together
Challenge: How to convert guest PASID to host PASID

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ENQCMD Instruction - Overview

- New instruction on Intel® Platforms
- Atomically submit a work with PASID
  - Obtains PASID from IA32_PASID MSR
  - Enqueue store 64B command to enqueue register in device MMIO
- IA32_PASID is managed by XSAVE as PASID supervisor state
- Non-Posted instruction which carries back a status
  - ZF flag indicates if the command was accepted by device
  - Allows user to retry

* Figure is from Intel® architecture instruction set extensions spec, see link in reference page page
ENQCMD Instruction - ENQCMDS

- ENQCMDS (Enqueue Command Supervisor)
  - Similar to ENQCMD
  - Used in kernel space only
  - Obtain PASID value from command data.
Support DMWr (Deferrable Memory Write) completer capability.

All switch ports and root ports have DMWr routing enabled.

Intel® Data Streaming Accelerator is the first device which supports ENQCMD
  - [https://lkml.org/lkml/2020/9/24/1056](https://lkml.org/lkml/2020/9/24/1056)
ENQCMD/ENQCMDS obtain guest PASID
Perform guest PASID to host PASID Translation
Enqueue store command data with host PASID to device
ENQCMD Virtualization - PASID Translation Support

• New feature in VMX on Intel® Platforms

• Use PASID Translation Table for guest PASID to host PASID translation

• Trigger VM-Exit if fails to translate guest PASID

* Figure is from Intel® architecture instruction set extensions spec, see link in reference page page
Manage PASID Translation Table in KVM

- Update translation per IO Address Space ID (IOASID) events
  - IOASID manages host PASID and its association to guest PASID
  - Monitor IOASID BIND/UNBIND events for translation update

Refer to “PASID Management in KVM” KVM Forum Session
PASID Translation Table is a per VM table shared by all VMCS

Modification must be a rendezvous operation
  • Kick all VCPUs into root mode and block VM entry until modification is done
  • Required by SDM 24.11.4, when modify data structure which is referenced by pointers in VMCS and controls non root mode operation.
Translation failure (VM-Exit) only happens with invalid guest PASID
  - Must be associated with a host PASID for DMA operation

Set the ZF = 1 to indicate the failure and skip the instruction
IA32_PASID MSR virtualization in KVM

- Passthrough IA32_PASID MSR
- Enable virtualization support for XSAVE PASID supervisor state component
Example – SVA Work Submission In Guest

- Prepare a Work Descriptor
- Submit by ENQCMD
  - PASID is translated automatically
  - Store Work Descriptor (GVA) + Host PASID to Device
  - Check ENQCMD instruction status
- Device performs DMA operation
  - GVA + Payload + Host PASID
- DMA address translation per RDI + PASID by IOMMU
  - GVA -> HPA
References

- Kernel Doc “Shared Virtual Addressing (SVA) with ENQCMD”- Documentation/x86/sva.rst by Ashok Raj <ashok.raj@intel.com>


- Intel® Scalable IOV: https://01.org/blogs/2019/assignable-interfaces-intel-scalable-i/o-virtualization-linux

Status

- ENQCMD native support: merged.
- IOASID extensions for notification: v3 submitted.
- ENQCMD virtualization support: will submit soon (internal review now)
  - TODO: Live migration support
Summary

• Dedicated Work Queue (DWQ) based on hard partitioning of resources, has scalability limitation in virtualization.

• Shared Work Queue (SWQ) with ENQCMD support allows more scalable usage in device virtualization, as same device interface can be shared by multiple users in host and VMs.

• Additional hardware support is required to support ENQCMD virtualization, e.g. PASID translation, XSAVE extension for PASID state and etc.